ABCD Production Plan

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1. Scope

This document describes the plans for producing the ABCD integrated circuit on the DMILL process. It will describe the flow of material from wafer fabrication through testing to hybrid assembly. The resources available to perform this work by the collaboration will also be itemized. Finally, a production schedule will be detailed.

2. Reference Documents

1. CERN Frame Contract No. B1124/EP DMILL Radiation Hard Foundry Services
2. Test System for ABCD3T Wafer Screening
3. Test Specification for ABCD3T Wafer Screening
4. ABCD3TA ASIC: QA

3. Material Flow

The ABCD integrated circuit (IC) has been designed to be processed on the rad-hard biCMOS process named DMILL. ATMEL has been licensed to fabricate wafers with this process and there now exists a Frame Contract between CERN and ATMEL to cover the fabrication of wafers for LHC projects. This Frame Contract will be the basis for purchases of ABCD wafers. Details concerning fabrication throughput times, delivery schedules and lead times for release orders are covered in the section of this document on Production Schedule and Run Rates.

A flow chart showing the overall material flow is shown in figure 1. Details of each operation are covered in figures 2-8.

ABCD Production Flow

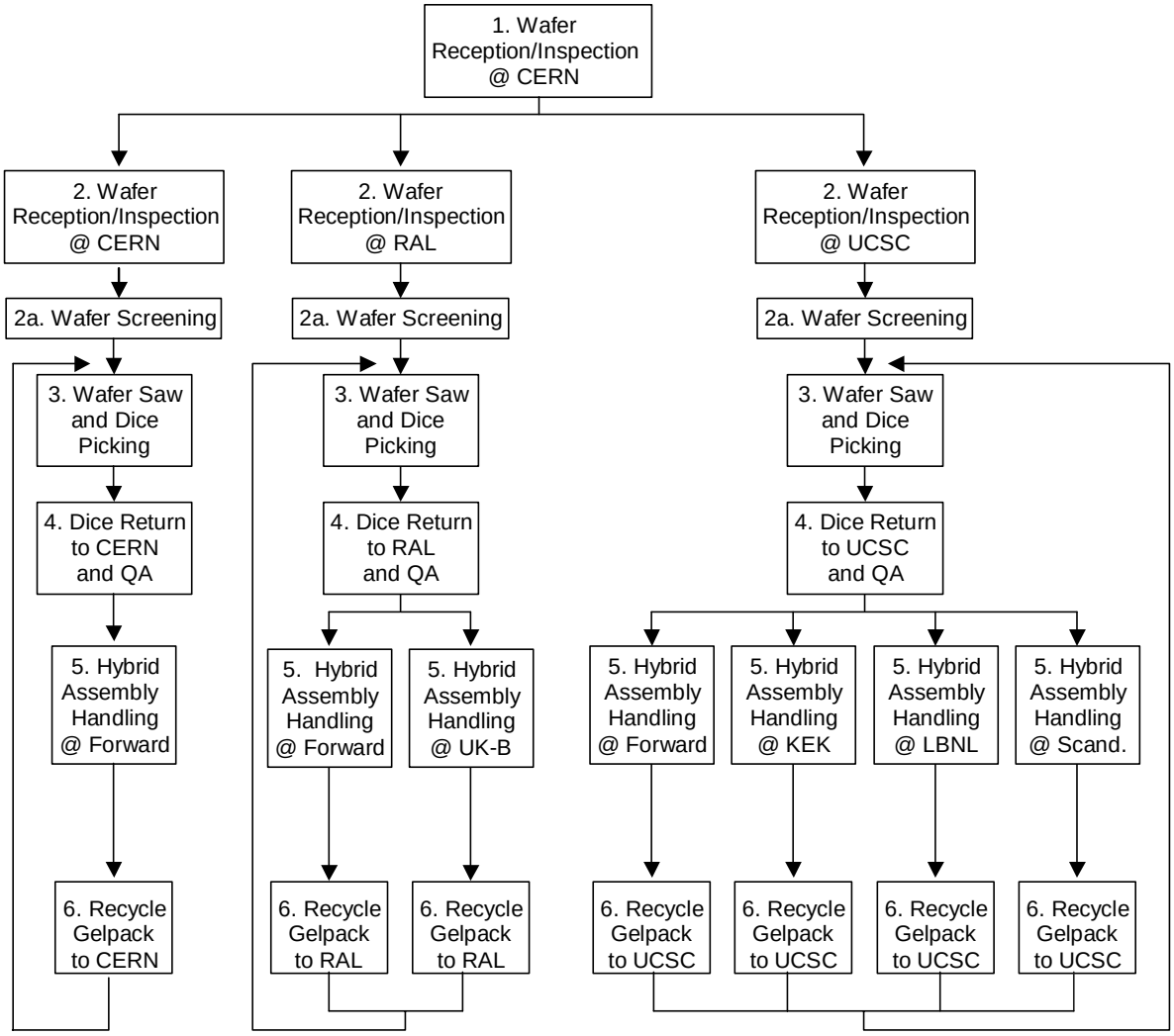

Figure 1: ABCD Production Flow

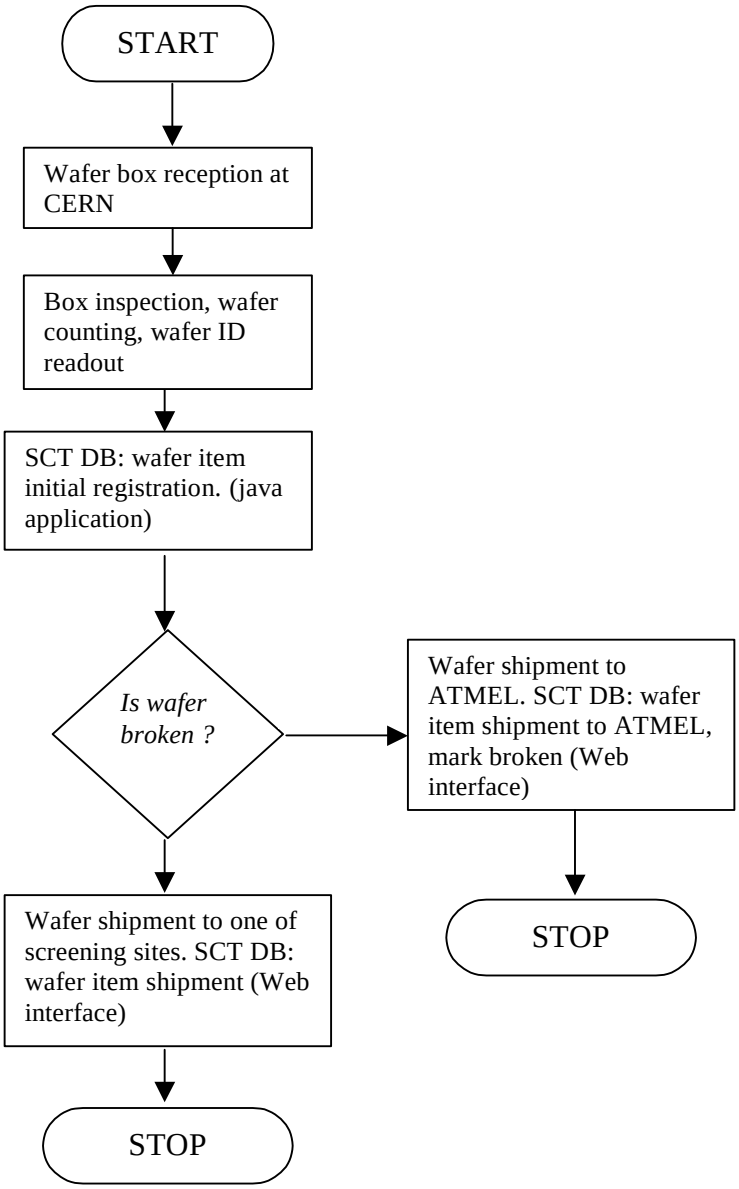

Figure 2: Step 1. Wafer Reception/Inspection at CERN

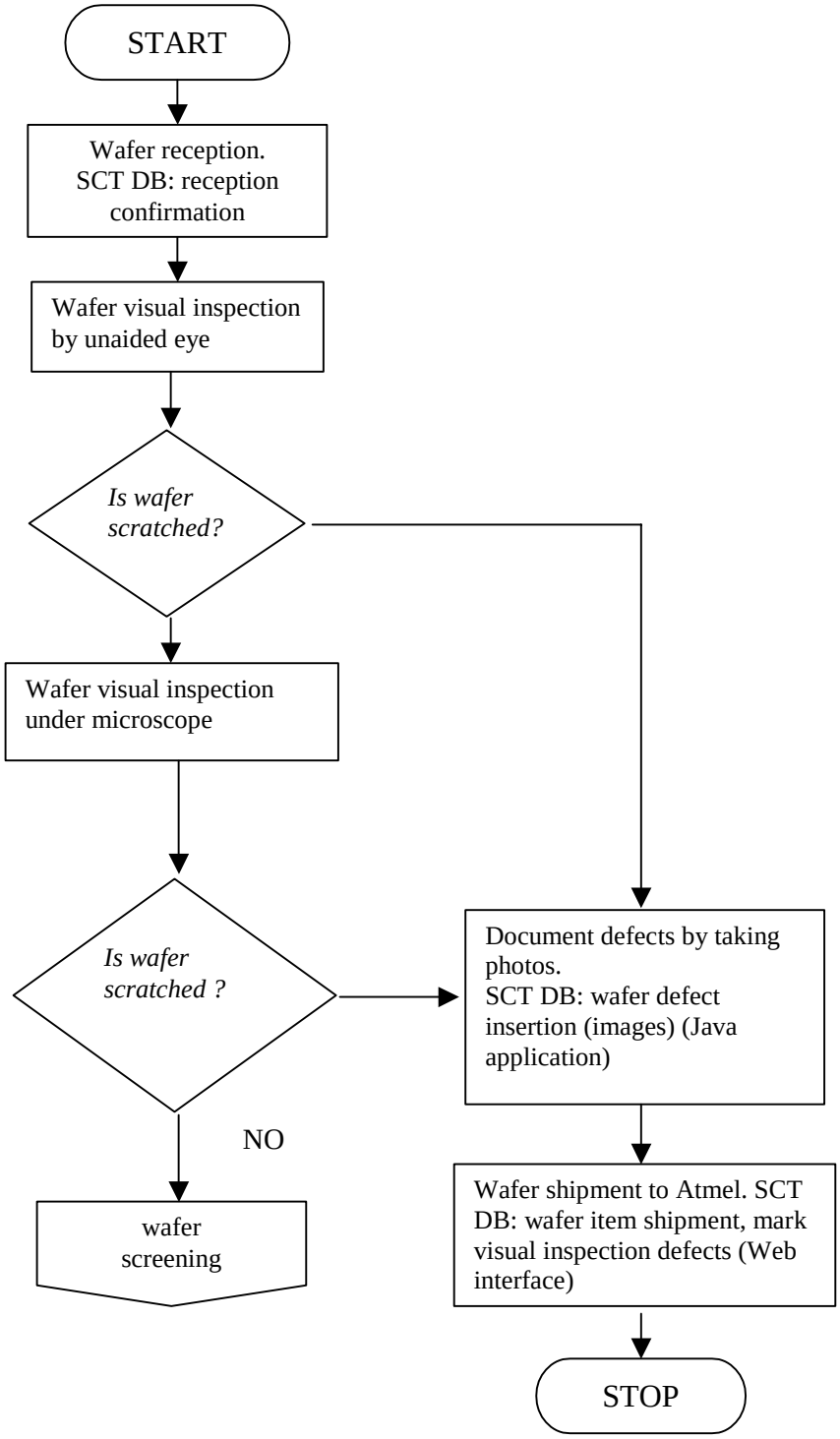

Figure 3: Step 2. Wafer Reception/Inspection at Screening Site

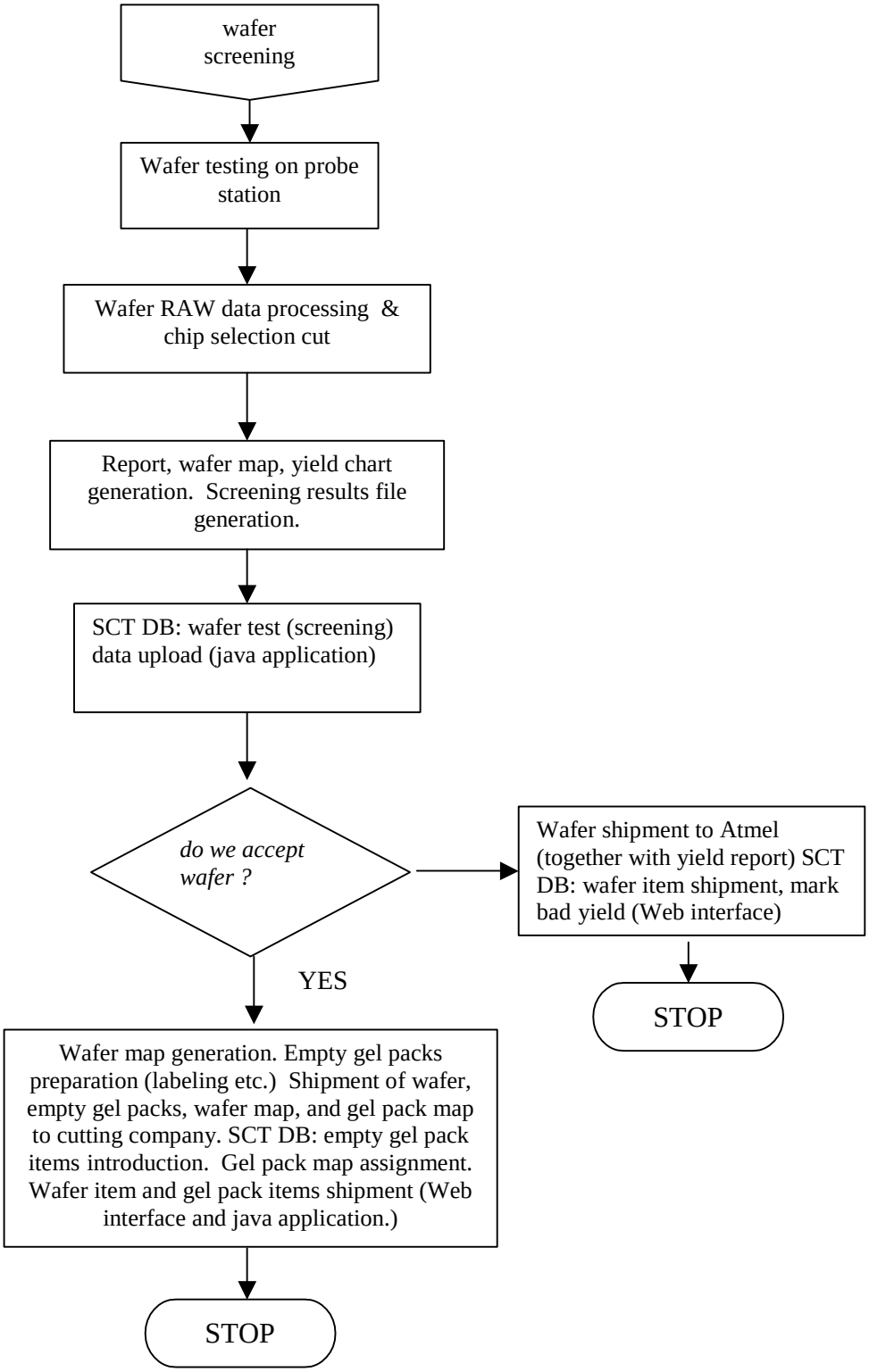

Figure 4: Step 2a. Wafer Screening

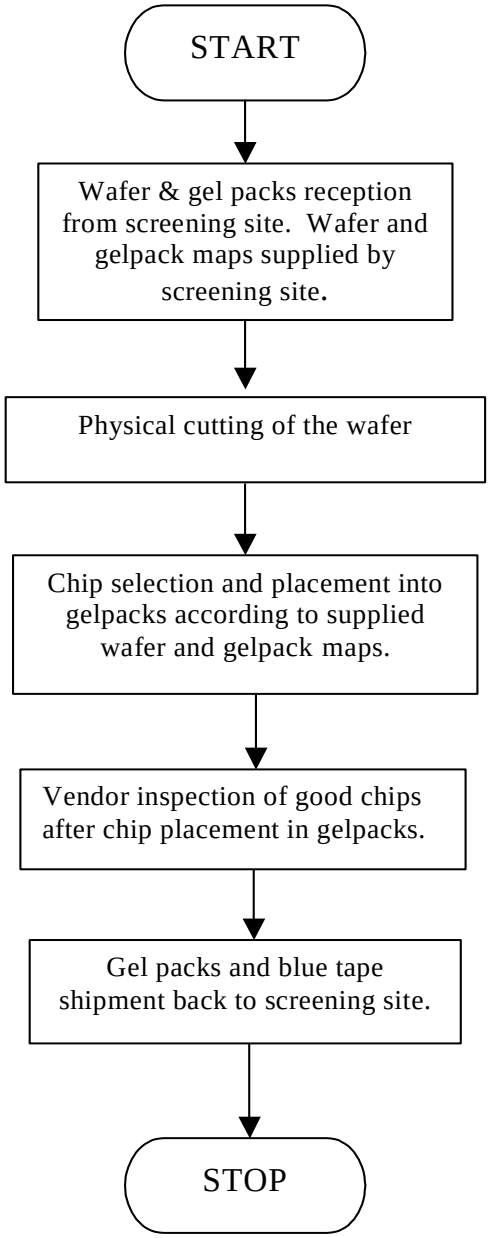

Figure 5: Step 3. Wafer Saw and Dice Picking

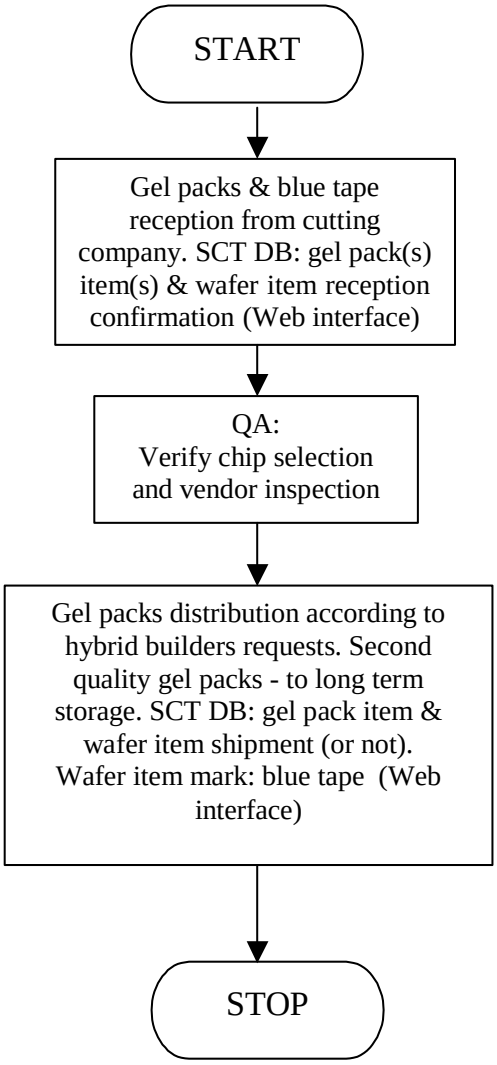

Figure 6: Step 4. Dice Return to Screening Site and QA

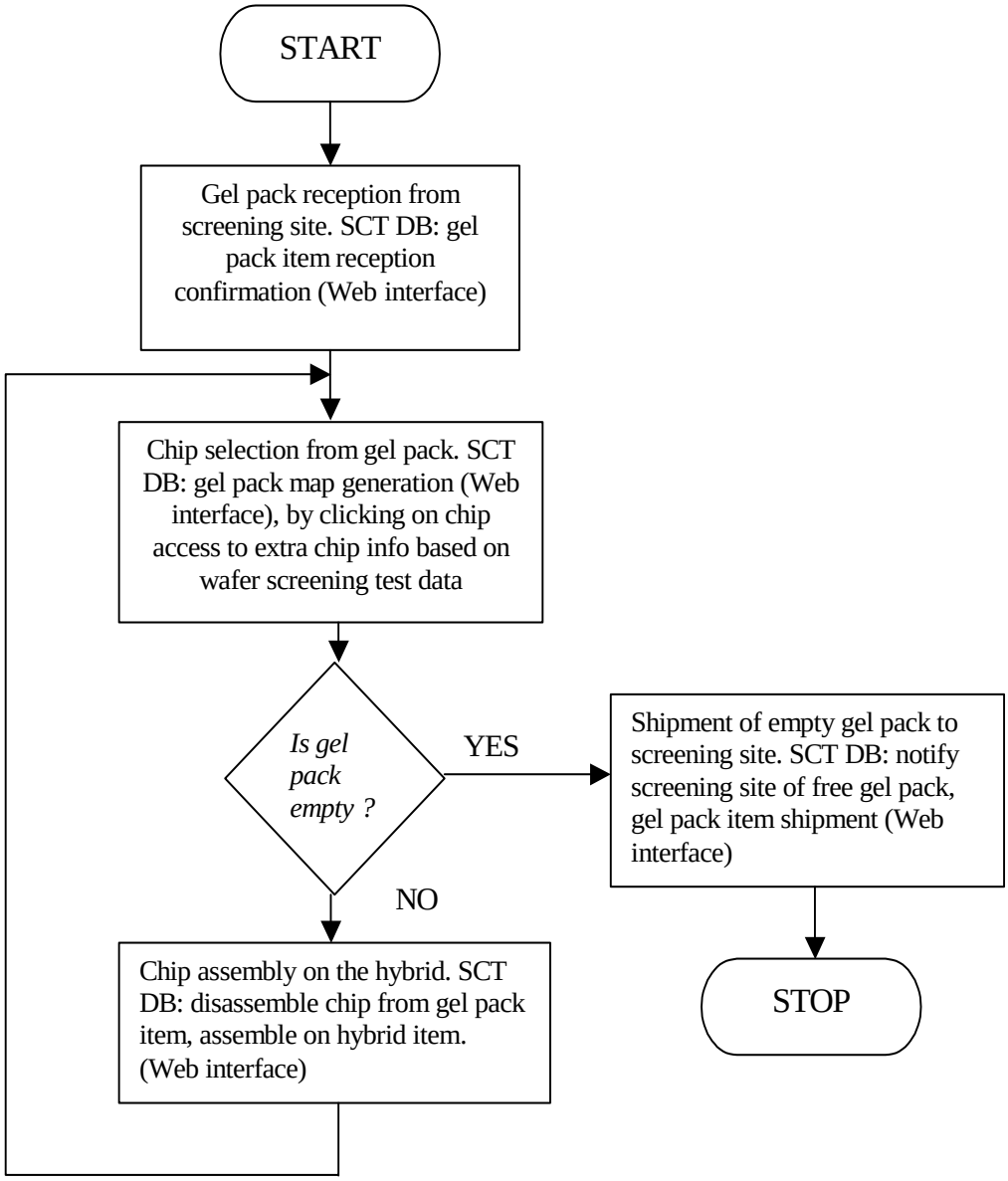

Figure 7: Step 5. Hybrid Assembly Handling

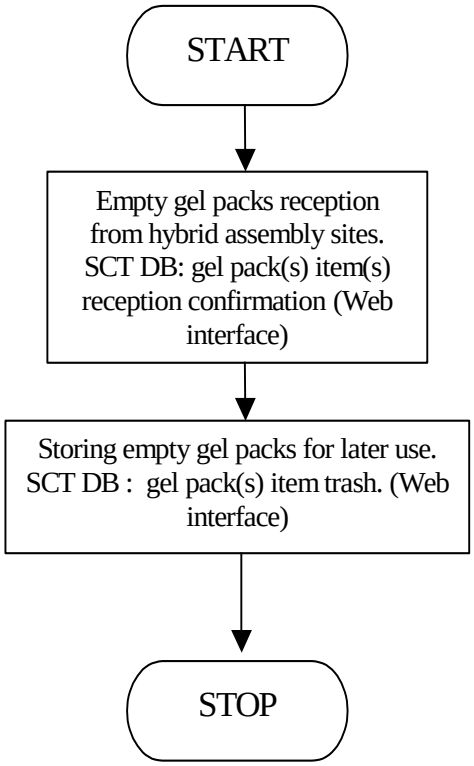

Figure 8: Step 6. Recycle Gel Pack to Screening Site

All wafers will be delivered to CERN as specified in the Frame Contract. This simplifies export rules and taxation issues. Wafers received at CERN will be inspected for breakage but a detailed visual inspection will be done by the individual test sites. This is mainly to spread the workload.

The wafers will be screened at one of three sites: CERN (25%), RAL (25%), and UCSC (50%). This is necessary in order to obtain sufficient resources to complete the screening task. Therefore, after the initial visual inspection and counting of wafers at CERN, 50% of the received wafers will be shipped to UCSC and 25% will be shipped to RAL.

At each of the three test sites, the wafers will be visually inspected for cracks, scratches or other surface defects. The acceptable wafers will be then tested using a probe station and computer controlled test system. This electrical test will test the full functionality of each IC on the wafer. Raw test data will be stored on disk and then analyzed by computer programs to make pass/fail decision on each chip. The chips will be binned into four categories: perfect, 1-bad-channel, 2-bad-channel, and bad.

Wafers will then be sent to a vendor for sawing. The vendors are contracted to saw each wafer and to "pick" the perfect chips placing them into gel packs. With each wafer sent to the saw vendor, a color

coded wafer map will be supplied which identifies the bin of each chip on the wafer. Another gel pack map will also be supplied that indicates where in the gel pack to place each perfect chip giving its row and column number from the wafer. As these maps are provided by the wafer test analysis software, the contents of each gel pack will be also recorded into the SCT database for future reference. The remaining chips (1-bad-channel, 2-bad-channel and bad) will be left on the blue tape used to hold the wafer during sawing. The vendor will visually inspect the perfect chips in the gel packs looking for cracks or chips along the chip edges. Any failing chips will be recorded but not removed from the gel packs. The filled gel packs and the remnant wafers will be returned to the test site. In the case of RAL, the vendor will store the remnant wafers.

Each test site will perform a sampling QA inspection of the gel packs and remnant wafers. The main goal is to verify correct selection of "good chips" from the wafer and the quality of the saw edges of the good chips. Final disposition of any cracked or chipped dice will also be made.

The gel packs with perfect chips will be shipped to the various hybrid assembly sites according to the agreed upon distribution plan. See the Production Schedule section below.

The remnant wafers which contain bad chips along with those found to have one or two bad channels will be stored at the test site institutions (RAL will store them at their saw vendor). The will be kept in cabinets flushed with dry air. There is no current plan to use the chips with one or two bad channels in the SCT but they will be kept in storage at least until the SCT construction is complete in case plans change.

A small sample number of chips will be taken from each wafer delivery for QA testing. This program is described in the QA Plan document.

4. Data Tracking

The entire flow of material will be tracked by the SCT Database. This is outlined in figures 2-8 as notes of "SCT DB: …". Web based tools will be used to record the shipment or reception of wafers and chips in gel packs. The wafer maps and gel pack maps used by the saw vendors to pick chips will be generated by Root macros and the database tools respectively. This will allow the database to track the location of chips in the gel packs by prescribing where the chips are to be packed.

5. Resources by Institution

It is the responsibility of each of the three test sites to provide the necessary resources, both equipment and personnel to accomplish the necessary work and to keep the schedule. The planned resources at each institution are given below.

Equipment:

	CERN	RAL	UCSC
Probe Station	1	1	1 (+1 planned)
Tester (set of PCBs)	2	2	3
Test Control Computer	1	1	1 (+1 planned)
Probe Cards	2	2	4
Offline Computer	ATLAS Cluster	ATLAS Cluster	ATLAS Cluster

Personnel (stated as Full Time Equivalent):

	CERN	RAL	UCSC
Technician	1	1	1
Test Operator	1	1	1.5
Admin Assistant		1	1

Since the test time for one wafer is targeted to be less than a single shift and the testers have been shown to work reliably unattended, each tester can run up to two wafers per day with a single shift by having the second wafer test started before the shift ends. The CERN and RAL systems plan to test one wafer per day but could increase to two if needed. The UCSC system will plan to test two wafers per day and could increase that to four once the second probe station and tester are added.

6. Production Schedule and Run Rates

The production schedule is achieved by balancing the wafer orders and fabrication throughput time with the rate of wafer screening at the three test sites and the requirements for chips of the hybrid assembly sites. The expected dates for release orders to start wafer fabrications and the subsequent wafer deliveries are shown in figure 9. Figures 10-12 show the wafer processing at each of the three test sites. Note that the column designation of "Forward" as a shipping destination is currently a place holder for the one or several institutes that will handle the forward hybrid assembly once those details are worked out. Figure 13 lists several of the assumptions used to work up the production schedule.

The assumed test rates at each site after a short ramp-up period are: CERN 1 wafer/day, RAL 1 wafer/day, UCSC 2 wafers/day. If the yield does not increase to the 26% level as indicated, ATMEL will have to deliver more wafers at faster rate (and lower cost) to keep the flow of good chips on schedule. Each test site will have to then accelerate its testing rate. That should be possible.

Week#	Date (last of Month)	Raw Wafers Released	Fabrication Released	WafersReceived by CERN	Expected Yield at Wafer Test
40	Sep-00	520			
		520			
31	Jul-01	675	520		
35	Aug-01	675	520	35	11.00%
39	Sep-01	675	520	35	11.00%
44	Oct-01	950	520	205	15.00%
48	Nov-01	950	675	405	15.00%
52	Dec-01	1,105	675	520	26.00%
5	Jan-02		675	520	26.00%
9	Feb-02		950	620	26.00%
13	Mar-02		1,105	675	26.00%
18	Apr-02			675	26.00%
22	May-02			675	26.00%
26	Jun-02			875	26.00%
31	Jul-02			1,105	26.00%
35	Aug-02				
39	Sep-02				
44	Oct-02				
48	Nov-02				
52	Dec-02				
5	Jan-03				
9	Feb-03				
13	Mar-03				
18	Apr-03				
22	May-03				
26	Jun-03				
31	Jul-03				
35	Aug-03				
39	Sep-03				
44	Oct-03				

Figure 9: Wafer Order and Delivery Plan

Week#	Date	At CERN						
	(last of Month)	Wfrs@CERN	WfrsTested	WfrsCut	GoodDice	DiceShpd	DiceTo:	Forward
40	Sep-00							
31	Jul-01							
35	Aug-01							
39	Sep-01	9	9	4	98			
44	Oct-01	9	9	9	251	251		251
48	Nov-01	51	21	13	348	251		251
52	Dec-01	101	31	31	915	585		585
5	Jan-02	130	51	41	1,295	915		915
9	Feb-02	130	71	61	2,055	1,675		1,675
13	Mar-02	155	91	81	2,816	2,436		2,436
18	Apr-02	169	116	106	3,906	3,386		3,386
22	May-02	169	136	126	5,223	4,564		4,564
26	Jun-02	194	156	146	6,541	5,882		5,882
31	Jul-02	238	181	171	8,189	7,530		7,530
35	Aug-02	276	201	191	9,507	8,848		8,848
39	Sep-02		221	211	10,824	10,165		10,165
44	Oct-02		246	236	12,472	11,813		11,813
48	Nov-02		266	256	13,790	13,131		13,131
52	Dec-02		276	276	15,108	14,449		14,449
5	Jan-03					15,108		15,108
9	Feb-03							
13	Mar-03							
18	Apr-03							
22	May-03							
26	Jun-03							
31	Jul-03							
35	Aug-03							
39	Sep-03							
44	Oct-03							

Figure 10: CERN Wafer Test Plan

Week#	Date	At RAL							
	(last of Month)	Wfrs@RAL	WfrsTested	WfrsCut	GoodDice	DiceShpd	DiceTo:	Forward	UK-B
40	Sep-00								
31	Jul-01								
35	Aug-01								
39	Sep-01	9	9	3	84				
44	Oct-01	9	9	9	251	251		122	128
48	Nov-01	51	21	13	362	251		122	128
52	Dec-01	101	29	29	849	585		286	299
5	Jan-02	130	49	39	1,229	849		414	434
9	Feb-02	130	69	59	1,990	1,609		785	822
13	Mar-02	155	84	79	2,750	2,370		1,156	1,210
18	Apr-02	169	109	99	3,510	3,130		1,527	1,599
22	May-02	169	129	119	4,828	4,169		2,035	2,129
26	Jun-02	194	149	139	6,146	5,487		2,678	2,803
31	Jul-02	238	174	164	7,793	7,134		3,482	3,644
35	Aug-02	276	194	184	9,111	8,452		4,125	4,317
39	Sep-02		214	204	10,429	9,770		4,768	4,990
44	Oct-02		239	229	12,076	11,417		5,572	5,832
48	Nov-02		259	249	13,394	12,735		6,215	6,505
52	Dec-02		269	269	14,712	14,053		6,858	7,178
5	Jan-03		276	276	15,173	14,712		7,180	7,514
9	Feb-03					15,173		7,405	7,750
13	Mar-03								
18	Apr-03								
22	May-03								
26	Jun-03								
31	Jul-03								
35	Aug-03								
39	Sep-03								
44	Oct-03								

Figure 11: RAL Wafer Test Plan

Week#	Date (last of Month)	At UCSC					DiceTo:	LBNL	Japan	Scand.	Forward
		Wfrs@UCSC	WfrsTested	WfrsCut	GoodDice	DiceShpd					
40	Sep-00										
31	Jul-01										
35	Aug-01										
39	Sep-01	18	12	4	112						
44	Oct-01	18	18	18	502	502		155	141	94	111
48	Nov-01	103	39	25	697	502		155	141	94	111
52	Dec-01	203	60	53	1,478	1,087		335	306	204	241
5	Jan-02	260	95	81	2,542	2,010		619	566	378	446
9	Feb-02	260	123	109	3,606	3,074		948	866	578	682
13	Mar-02	310	163	143	4,899	4,139		1,276	1,166	778	919
18	Apr-02	338	213	193	6,800	6,039		1,861	1,702	1,135	1,341
22	May-02	338	253	233	9,157	7,839		2,416	2,209	1,473	1,740
26	Jun-02	388	293	273	11,793	10,475		3,228	2,952	1,968	2,325
31	Jul-02	475	343	323	15,087	13,769		4,244	3,880	2,587	3,057
35	Aug-02	553	383	363	17,723	16,405		5,056	4,623	3,082	3,642
39	Sep-02		423	403	20,359	19,041		5,869	5,366	3,577	4,227
44	Oct-02		473	453	23,654	22,336		6,884	6,294	4,196	4,959
48	Nov-02		513	493	26,289	24,971		7,697	7,037	4,691	5,544
52	Dec-02		543	533	28,925	27,607		8,509	7,780	5,186	6,129
5	Jan-03		553	553	30,243	30,243		9,321	8,522	5,682	6,714
9	Feb-03										
13	Mar-03										
18	Apr-03										
22	May-03										
26	Jun-03										
31	Jul-03										
35	Aug-03										
39	Sep-03										
44	Oct-03										

Figure 12: UCSC Wafer Test Plan

Assumptions:	
PRR	*04-Jul-01*
First Production Release	*09-Jul-01*
Number of days for first wafers	*140*
# of raw dice per wafer	*256*
Yield at Saw + Pack	*99.00%*
Total # of Dice Needed	*60,231*
Wafer Delivery Dates:	
13-Aug-01	*35*
15-Oct-01	*105*
29-Oct-01	*205*
12-Nov-01	*305*
26-Nov-01	*405*
10-Dec-01	*520*
25-Feb-02	*620*
11-Mar-02	*675*
3-Jun-02	*775*
17-Jun-02	*875*
1-Jul-02	*950*
15-Jul-02	*1105*

Total # of Modules in Exp	*4,088*
US Modules in Exp	*630*
US % of Total Modules	*15.41%*
Japan Modules in Exp	*576*
Japan % of Total Modules	*14.09%*
Scandinavia Modules in Exp	*384*
Scandinavia % of Total Modules	*9.39%*
UK-B Modules in Exp	*522*
UK-B % of Total Modules	*12.77%*
Forward Modules in Exp	*1,976*
Forward % of Total Modules	*48.34%*
Forward % of Total Modules From CERN	*25.00%*
Forward % of Total Modules From RAL	*12.20%*
Forward % of Total Modules From UCSC	*11.10%*

Figure 13: Production Plan Assumptions